IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. **(Currently Amended)** A method, comprising:

monitoring a state of an application running in a system, including monitoring one or more buffers associated with the application;

monitoring a machine state of the system, including determining the availability of configurable hardware components in the system, wherein the configurable hardware components include at least a processor **that performs simultaneous multi-threading** and a buffer;

coordinating dispatch of ~~one or more~~ **a plurality of** threads in the system at least in part to increase execution overlap **of the threads**, wherein at least one **of the** thread**s** is associated with the application;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the ~~one or more~~ threads; and

dynamically adjusting the buffer size based at least on the state of the application and the state of the ~~one or more~~ threads in the system.

2. **(Currently Amended)** The method of claim 1, wherein a thread includes one or more activities, and wherein said coordinating dispatch of the ~~one or more~~ threads in the system includes assessing execution readiness of the one or more activities.

3. **(Currently Amended)** The method of claim 2, wherein said coordinating dispatch of the ~~one or more~~ threads in the system includes delaying a ready-to-be-dispatched activity from being dispatched.

4. (Original) The method of claim 3, wherein a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second

activities can be dispatched together, and wherein the first and second activities are from one or more applications.

5-6. (Cancelled)

7. (Previously Presented) The method of claim 6, wherein the configurable hardware components further include, hardware buffers, memory, cache, arithmetic logic unit (ALU), and registers in the system.

8-9. (Cancelled)

10. (Previously Presented) The method of claim 7, wherein adjusting the voltage applied to the processor includes powering on or powering off at least a portion of circuitry in the system.

11. (Original) The method of claim 1, wherein said monitoring the one or more buffers associated with the application includes monitoring buffer fullness levels of the one or more buffers.

12. (Original) The method of claim 11, wherein said monitoring the buffer fullness levels includes, for each buffer associated with the application, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark.

13. (Original) The method of claim 12, wherein said comparing is to determine buffer overflow and buffer underflow conditions.

14. (**Currently Amended**) A computer readable storage medium containing executable instructions which, when executed in a processing system, causes the processing system to perform a method comprising:

monitoring a state of an application running in a system, including monitoring one or more buffers associated with the application;

monitoring a machine state of the system, including determining the availability of configurable hardware components in the system, wherein the configurable hardware components include at least a processor **that performs simultaneous multi-threading** and a buffer;

coordinating dispatch of ~~one or more~~ **a plurality of** threads in the system at least in part to increase execution overlap **of the threads**, wherein at least one **of the** thread**s** is associated with the application;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the ~~one or more~~ threads; and

dynamically adjusting the buffer size based at least on the state of the application and the state of the ~~one or more~~ threads in the system.

15. (**Currently Amended**) The computer readable storage medium of claim 14, wherein said coordinating the dispatch of the ~~one or more~~ threads in the system includes delaying a ready-to-be-dispatched thread from being dispatched.

16-18. (Cancelled)

19. (Previously Presented) The computer readable storage medium of claim 14, wherein said monitoring the buffer fullness levels includes, for each buffer associated with the application, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark.

20-38. (Cancelled)

39. (**Currently Amended**) A system, comprising:

a memory to store data and instructions;

a processor coupled to said memory on a bus, said processor operable to perform instructions, said processor comprising:

a bus unit to receive a sequence of instructions from said memory;

an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions, said sequence of instructions to cause said execution unit to:

monitor a state of an application running in a system, including monitoring buffer fullness levels of one or more buffers associated with the application;

monitor~~ing~~ a machine state of the system, including determining the availability of configurable hardware components in the system, wherein the configurable hardware components include at least a processor **that performs simultaneous multi-threading** and a buffer;

coordinate dispatch of ~~one or more~~ **a plurality of** threads in the system at least in part to increase execution overlap **of the threads**, wherein at least one thread is associated with the application;

dynamically adjust one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the ~~one or more~~ threads; and

dynamically adjusting the buffer size based at least on the state of the application and the state of the ~~one or more~~ threads in the system.

40. (**Currently Amended**) The system of claim 39, wherein said coordinating the dispatch of the ~~one or more~~ threads in the system includes delaying a ready-to-be-dispatched thread from being dispatched.

41. (Previously Presented) The system of claim 39, further comprising instructions to cause said

execution unit to monitor a machine state of the system, wherein said monitoring the machine state includes:

determining resources available in the system, and

increasing or decreasing the configurable hardware components available in the system based on the state of the application and the state of the one or more threads in the system.

42-43. (Cancelled)

44. (**Currently Amended**) A system, comprising:

a multi-threading processor; and

a resource manager coupled to the multi-threading processor, the resource manager is to monitor states of an application running in the system, the states of the application including buffer fullness levels of one or more buffers used by the application, the resource manager is to further monitor states of ~~one or more~~ **a plurality of** threads in the system for execution readiness, wherein the resource manager is to increase or decrease resources available in the system depending on the state of the application and/or the states of the ~~one or more~~ threads in the system.

45. (Original) The system of claim 44, wherein the resource manager is to change the execution readiness of a thread from a ready state to a queued state to increase subsequent thread execution overlap with execution of another thread.

46. (Original) The system of claim 45, wherein the resource manager is to change the execution readiness of a thread from a ready state to a queued state to increase subsequent system idle time when there is no thread execution.

47. (Original) The system of claim 46, wherein the resource manager is to increase or decrease the resources available in the system to avoid buffer underflow or overflow conditions to occur to the one or more buffers.

48. (**Currently Amended**) An apparatus, comprising:

a processor capable of simultaneous multi-threading , the processor having

logic to monitor states of an application running in a system, the states of the application including buffer fullness levels of one or more buffers used by the application;

logic to monitor states of ~~one or more~~ **a plurality of** threads in the system for execution readiness;

logic to adjust resources available in the system depending on the state of the application and/or the states of the ~~one or more~~ threads in the system; and

a memory to store the logic.

49. (Original) The apparatus of claim 48, further comprising:

logic to change the execution readiness of a thread from a ready state to a queued state when it is determined that there is no other thread running or ready to be dispatched.

50. (Original) The apparatus of claim 48, wherein the logic to adjust the available resources in the system includes logic to determine if the buffer fullness levels of one or more buffers are in a critical stage.